AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A liquid crystal display device with a multi-timing controller, comprising:

a liquid crystal display panel having a display standard;

an interface receiving a timing data inputted from the exterior thereof and a control signal corresponding to the display standard;

a timing controller for latching and outputting the timing data inputted from the interface, and for generating and outputting timing signals for driving the liquid crystal display panel based on the control signal; and

a driving circuit for receiving the timing signals outputted from the timing controller to display a picture corresponding to the display standard,

wherein said timing controller includes a decoder and a timing generator,

wherein timing generation information corresponding to a plurality of display standards is stored by the decoder,

wherein the decoder outputs, to the timing generator, timing information corresponding to the timing data,

wherein the timing generator outputs timing signals corresponding to the timing information and the control signal, [[~~and~~]]

wherein the timing generator includes a first controller for generating the timing signal corresponding to the timing information selected from the decoder and a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity of the liquid crystal provided on the liquid crystal display panel and a gate drive starting signal for notifying a first drive line of a field from one vertical synchronizing signal[[~~,~~]],

a third controller for generating a signal informing a sampling start of a data and a source sampling clock for latching a data at the rising or falling edge during one horizontal synchronization period,

a forth controller for deforming a gate output enable signal generated from the first controller by making the gate output enable signal into a high state during a certain time so as to prevent a latch-up badness in which all the outputs of a gate drive integrate circuit goes to a high state, thereby disabling the gate drive integrated circuit, and

a fifth controller for always equally keeping the polarity of the horizontal/vertical synchronizing signal.

2. (Previously Presented) The liquid crystal display device as claimed in claim 1, further comprising a dip switch for selecting the timing data corresponding to the display standard.

3. (Previously Presented) The liquid crystal display device as claimed in claim 1, wherein the decoder consists of a memory for storing a certain timing information and a multiplexor for selecting any one of the timing information stored in the memory.

4. (Canceled)

5. (Previously Presented) The liquid crystal display device as claimed in claim 1, wherein the first controller includes:

a first counter for receiving the horizontal synchronizing signal inputted from the fifth controller and the first timing information inputted from the decoder to count the timing information during two horizontal periods and thus output a first count value;

a subtractor for subtracting the timing information from the first count value to output a reference timing signal;

a second counter for counting the timing information every period of the horizontal synchronizing signal to output a second count value for the current horizontal period;

a first comparator for comparing the second count value with the reference timing signal to output a first selection timing signal;

a third counter for receiving the first selection timing signal as an initializing signal to count the reference clock during one horizontal period and thus output a third count value;

a second comparator for receiving the third count value to compare it with a second timing information inputted from the decoder, thereby outputting a second selection timing signal when the two input values are equal;

a third comparator for receiving the third count value to compare it with a third timing information inputted from the decoder, thereby outputting a third selection timing signal when the two input values are equal;

a fourth comparator for comparing the second count value with a fourth timing information inputted from the decoder to output a fourth selection timing signal when the two input values are equal;

a fifth comparator for comparing the second count value with a fifth timing information inputted from the decoder to output a fifth selection timing signal when the two input values are equal; and

a sixth comparator for comparing the second count value with a sixth timing information inputted from the decoder to output a sixth reference timing signal when the two input values are equal.

6. (Previously Presented) The liquid crystal display device as claimed in claim 2, wherein the display standard is selected from any one of SVGA, XGA, SXGA, UXGA, and VGA display standards.

7. (Currently Amended) A multi-timing controller, comprising:

a decoder for storing timing generation information corresponding to a plurality of display standards, wherein the decoder is connected to a source outputting timing data; and

a timing generator connected to an output of the decoder and to a source outputting a control signal and to a source outputting a control signal corresponding to one of the plurality of display standards, wherein the timing generator outputs, to a display device, timing signals corresponding to an output of the decoder and the control signal,

wherein the timing generator includes a first controller ~~first controller~~ that generates the timing signal output by the timing generator and a second controller that generates a polarity inversion signal indicating a driving voltage polarity and a starting signal for notifying a first drive line of a field from one vertical synchronizing signal, and

wherein the first controller includes:

a first counter for receiving a horizontal synchronizing signal and the first timing information inputted from the decoder to count the timing information during two horizontal periods and thus output a first count value;

a subtractor for subtracting the timing information from the first count value to output a reference timing signal;

a second counter for counting the timing information every period of the horizontal synchronizing signal to output a second count value for the current horizontal period;

a first comparator for comparing the second count value with the reference timing signal to output a first selection timing signal;

a third counter for receiving the first selection timing signal as an initializing signal to count the reference clock during one horizontal period and thus output a third count value;

a second comparator for receiving the third count value to compare it with a second timing information inputted from the decoder, thereby outputting a second selection timing signal when the two input values are equal.

8. (Previously Presented) The multi-timing controller of claim 7, wherein the decoder includes a memory and a multiplexor.

9. (Previously Presented) The multi-timing controller of claim 7, wherein the timing generator includes a third controller, a fourth controller, and a fifth controller, wherein:

the first controller is connected to an output of the fifth controller;

the second controller is connected to an output of the fourth controller;

the third controller is connected to an output of the second controller and generates a signal informing a sampling start of a data and a source sampling clock for latching a data at the rising or falling edge during one horizontal synchronization period;

the fourth controller is connected to an output of the first controller and deforms a gate output enable signal generated by the first controller, thereby making the gate output enable signal into a high state during a certain time in which all the outputs of a driver circuit are in a high state, thereby disabling the driver circuit; and

the fifth controller maintains the polarity of the control signal.

10. (Currently Amended) The liquid crystal display device as claimed in claim 9, wherein the first controller includes:

~~a first counter for receiving the horizontal synchronizing signal inputted from the fifth controller and the first timing information inputted from the decoder to count the timing information during two horizontal periods and thus output a first count value;~~

~~a subtractor for subtracting the timing information from the first count value to output a reference timing signal;~~

~~a second counter for counting the timing information every period of the horizontal synchronizing signal to output a second count value for the current horizontal period;~~

~~a first comparator for comparing the second count value with the reference timing signal to output a first selection timing signal;~~

~~a third counter for receiving the first selection timing signal as an initializing signal to count the reference clock during one horizontal period and thus output a third count value;~~

~~a second comparator for receiving the third count value to compare it with a second timing information inputted from the decoder, thereby outputting a second selection timing signal when the two input values are equal;~~

a third comparator for receiving the third count value to compare it with a third timing information inputted from the decoder, thereby outputting a third selection timing signal when the two input values are equal;

a fourth comparator for comparing the second count value with a fourth timing information inputted from the decoder to output a fourth selection timing signal when the two input values are equal;

a fifth comparator for comparing the second count value with a fifth timing information inputted from the decoder to output a fifth selection timing signal when the two input values are equal; and

a sixth comparator for comparing the second count value with a sixth timing information inputted from the decoder to output a sixth reference timing signal when the two input values are equal.